IN THE CLAIMS:

1. (Canceled)

2. (Currently Amended) ~~The phase locked loop circuit as claimed in claim 1,~~ A phase locked loop circuit comprising:

a phase control unit, a frequency control unit and an oscillator;

a first feedback circuit which feeds back an output of said oscillator to said oscillator through said phase control unit which operates for integral control; and

a second feedback circuit which feeds back the output of said oscillator to said oscillator through said frequency control unit which operates for proportional control,

wherein said first feedback circuit and said second feedback circuit are connected to said oscillator at all times so as to carry out the integral control and the proportional control continuously, and

wherein said second feedback circuit includes a first converter circuit for conversion of said first clock signal into a first current, a second converter circuit for conversion of said second clock signal to a second current, and a current adder circuit for adding said first current and said second current together.

3. (Currently Amended) ~~The phase locked loop circuit as claimed in claim 1,~~ A phase locked loop circuit comprising:

a phase control unit, a frequency control unit and an oscillator;

a first feedback circuit which feeds back an output of said oscillator to said oscillator through said phase control unit which operates for integral control; and

a second feedback circuit which feeds back the output of said oscillator to said oscillator through said frequency control unit which operates for proportional control,

wherein said first feedback circuit and said second feedback circuit are connected to said oscillator at all times so as to carry out the integral control and the proportional control continuously, and

wherein said second feedback circuit includes a first converter circuit for conversion of said first clock signal to a first voltage, a second converter circuit for conversion of said second clock signal to a second voltage, and a voltage adder circuit for adding said first voltage and said second voltage together.

4. and 5. (Canceled)

6. (Currently Amended) ~~The phase locked loop circuit as claimed in claim 4 or 5,~~ A phase locked loop circuit comprising:

a first control signal generator unit responsive to receipt of an input signal, for generating a first control signal for integral control of an output signal;

a second control signal generator unit for generating based on the input signal a second control signal for proportional control of an output signal;

an oscillator responsive to the first and second control signals for outputting a clock signal;

a first feedback circuit for feeding back an output of said oscillator to said oscillator through said first control signal generator unit; and

a second feedback circuit for feeding back the output of said oscillator to said oscillator through said second control signal generator unit,

wherein said first feedback circuit and said second feedback circuit are connected to said oscillator at all times so as to operate continuously, and

wherein said ~~first~~ second control signal generator unit includes a first converter circuit for conversion of an input signal to a first current, a second converter circuit for conversion of an output signal to a second current, and a current adder circuit for adding together said first current and said second current.

7. (Currently Amended) ~~The phase locked loop circuit as claimed in claim 4 or 5,~~ A phase locked loop circuit comprising:

a first control signal generator unit responsive to receipt of an input signal, for generating a first control signal for integral control of an output signal;

a second control signal generator unit for generating based on the input signal a second control signal for proportional control of an output signal;

an oscillator responsive to the first and second control signals for outputting a clock signal;

a first feedback circuit for feeding back an output of said oscillator to said oscillator through said first control signal generator unit; and

a second feedback circuit for feeding back the output of said oscillator to said oscillator through said second control signal generator unit,

wherein said first feedback circuit and said second feedback circuit are connected to said oscillator at all times so as to operate continuously, and

wherein said ~~first~~ second control signal generator unit includes a first converter circuit for conversion of an input signal to a first voltage, a second converter circuit for conversion of an output signal to a second voltage, and a voltage adder circuit for adding together said first voltage and said second voltage.

8. (Previously Presented) The phase locked loop circuit as claimed in claim 6, wherein said first and second converter circuits include a charging/discharging circuit having a capacitor and a CMOS inverter for performing charging and discharging on the basis of a signal as input thereto, and a current mirror filter with a plurality of current mirror circuits folded for connection together.

9.-23. (Canceled)

24. (Previously Presented) A phase locked loop circuit comprising:

a phase comparator circuit for outputting a phase difference signal from anyone of two output terminals in accordance with a phase difference between two signals as input thereto;

a charge pump circuit responsive to receipt of the phase difference signal from said phase comparator circuit for permitting charging and discharging of a capacitor to generate a control voltage signal; and

an oscillator responsive to the control voltage signal from said charge pump circuit for adjusting a transmission frequency, wherein said charge pump circuit includes a first current switch circuit for charging up said capacitor in deference to the phase difference signal as output from one output terminal of said phase comparator circuit, and a second current switch circuit for discharging said capacitor in response to the phase difference signal as output from a remaining one of the output terminals of said phase comparator circuit, and

wherein said first and second current switch circuits comprise a current switch using a CMOS inverter with a control electrode forward-biased and a complementary paired output voltage switch for driving said current switch with an output connected to a low voltage-side electrode of said current switch.

25. (Canceled)

26. (Previously Presented) The phase locked loop circuit as claimed in claim 7, wherein said first and second converter circuits include a charging/discharging circuit having a capacitor and a CMOS inverter for performing charging and discharging on the basis of a signal as input thereto, and a current mirror filter with a plurality of current mirror circuits connected together in a folded fashion.

27.-31. (Canceled)

32. (Previously Presented) A phase locked loop circuit comprising:

a first feedback circuit operatively responsive to receipt of a first clock signal, for generating a second clock signal synchronized in phase with the first clock signal; and

a second feedback circuit for generation of said second clock signal substantially equal in frequency to said first clock signal as input thereto, said second feedback circuit comprising:

a first converter for conversion of said first clock signal into a first current;

a second converter for conversion of said second clock signal to a second current; and

an adder for adding said first current and said second current together.

33. (Previously Presented) A phase locked loop circuit comprising:

a first feedback circuit operatively responsive to receipt of a first clock signal, for generating a second clock signal synchronized in phase with the first clock signal; and

a second feedback circuit for generation of said second clock signal substantially equal in frequency to said first clock signal as input thereto, said second feedback circuit comprising:

a first converter for conversion of said first clock signal into a first voltage;

a second converter for conversion of said second clock signal to a second voltage; and

an adder for adding said first voltage and said second voltage together.

34. (Previously Presented) A phase locked loop circuit comprising:

a first control signal generator unit responsive to receipt of an input signal, for generating a first control signal for integral control of an output signal;

a second control signal generator unit for generating, based on the input signal, a second control signal for proportional control of an output signal; and

an oscillator responsive to the first and second control signals, for outputting a clock signal;

wherein said first control signal generator unit includes a first converter circuit for conversion of an input signal to a first current, a second converter circuit for conversion of an output signal to a second current, and a current adder circuit for adding together said first current and said second current.

35. (Previously Presented) A phase locked loop circuit comprising:

a first control signal generator unit responsive to receipt of an input signal, for generating a first control signal for integral control of an output signal;

a second control signal generator unit for generating, based on the input signal, a second control signal for proportional control of an output signal; and

an oscillator responsive to the first and second control signals for outputting a clock signal;

wherein said first control signal generator unit uses a difference in phase between said input signal and said output signal to generate said first control signal, whereas said second control signal generator unit uses a difference in frequency between said input signal and said output signal to generate said second control signal; and

wherein said first control signal generator unit includes a first converter circuit for conversion of an input signal to a first current, a second converter circuit for conversion of an output signal to a second current, and a current adder circuit for adding together said first current and said second current.

36. (Previously Presented) The phase locked loop circuit as claimed in claim 34, wherein said first and second converter circuits include a charging/discharging circuit having a capacitor and a CMOS inverter for performing charging and discharging on the basis of a signal as input thereto, and a current mirror filter with a plurality of current mirror circuits folded for connection together.

37. (Previously Presented) The phase locked loop circuit as claimed in claim 35, wherein said first and second converter circuits include a charging/discharging circuit having a capacitor and a CMOS inverter for performing charging and discharging on the basis of a signal as input thereto, and a current mirror filter with a plurality of current mirror circuits folded for connection together.

38. (Previously Presented) A phase locked loop circuit comprising:

a first control signal generator unit responsive to receipt of an input signal, for generating a first control signal for integral control of an output signal;

a second control signal generator unit for generating, based on the input signal, a second control signal for proportional control of an output signal; and

an oscillator responsive to the first and second control signals, for outputting a clock signal;

wherein said first control signal generator unit includes a first converter circuit for conversion of an input signal to a first voltage, a second converter circuit for conversion of an output signal to a second voltage, and a voltage adder circuit for adding together said first voltage and said second voltage; and

wherein said first and second converter circuits include a charging/discharging circuit having a capacitor and a CMOS inverter for performing charging and discharging on the basis of a signal as input thereto, and a current mirror filter with a plurality of current mirror circuits connected together in a folded fashion.

39. (New) The phase locked loop circuit as claimed in claim 6, wherein said first control signal generator unit uses a difference in phase between said input signal and said output signal to generate said first control signal, whereas said second control signal generator unit uses a difference in frequency between said input signal and said output signal to generate said second control signal.

40. (New) The phase locked loop circuit as claimed in claim 7, wherein said first control signal generator unit uses a difference in phase between said input signal and said output signal to generate said first control signal, whereas said second control signal generator unit uses a difference in frequency between said input signal and said output signal to generate said second control signal.

41. (New) An information processing apparatus comprising:

a clock generator unit;

a clock control unit for controlling the clock signal as output from said clock generator unit; and

a logic unit for processing data based on the clock signal as generated by said clock generator unit,

wherein said clock generator unit comprising:

a phase control unit, a frequency control unit and an oscillator;

a first feedback circuit which feeds back an output of said oscillator to said oscillator through said phase control unit which operates for integral control; and

a second feedback circuit which feeds back the output of said oscillator to said oscillator through said frequency control unit which operates for proportional control,

wherein said first feedback circuit and said second feedback circuit are connected to said oscillator at all times so as to carry out the integral control and the proportional control continuously, and

said second feedback circuit includes a first converter circuit for conversion of said first clock signal into a first current, a second converter circuit for conversion of said second clock signal to a second current, and a current adder circuit for adding said first current and said second current together.

42. (New) An information processing apparatus comprising:

a clock generator unit;

a clock control unit for controlling the clock signal as output from said clock generator unit; and

a logic unit for processing data based on the clock signal as generated by said clock generator unit,

wherein said clock generator unit comprising:

a phase control unit, a frequency control unit and an oscillator;

a first feedback circuit which feeds back an output of said oscillator to said oscillator through said phase control unit which operates for integral control; and

a second feedback circuit which feeds back the output of said oscillator to said oscillator through said frequency control unit which operates for proportional control,

wherein said first feedback circuit and said second feedback circuit are connected to said oscillator at all times so as to carry out the integral control and the proportional control continuously, and

said second feedback circuit includes a first converter circuit for conversion of said first clock signal to a first voltage, a second converter circuit for conversion of

said second clock signal to a second voltage, and a voltage adder circuit for adding said first voltage and said second voltage.

43. (New) An information processing apparatus comprising:

a clock generator unit;

a clock control unit for controlling the clock signal as output from said clock generator unit; and

a logic unit for processing data based on the clock signal as generated by said clock generator unit,

wherein said clock generator unit comprising:

a first control signal generator unit responsive to receipt of an input signal, for generating a first control signal for integral control of an output signal;

a second control signal generator unit for generating based on the input signal a second control signal for proportional control of an output signal:

an oscillator responsive to the first and second control signals for outputting a clock signal;

a feedback circuit for feeding back an output of said oscillator to said oscillator through said first control signal generator unit; and

a second feedback circuit for feeding back an output of said oscillator to said oscillator through said second control signal generator unit,

wherein said first feedback circuit and said second feedback circuit are connected to said oscillator at all times so as to operate continuously, and

said second control signal generator unit includes a first converter circuit for conversion of an input signal to a first current, a second converter circuit for conversion of an output signal to a second current, and a current adder circuit for adding together said first current and said second current.

44. (New) An information processing apparatus comprising:

a clock generator unit;

a clock control unit for controlling the clock signal as output from said clock generator unit; and

a logic unit for processing data based on the clock signal as generated by said clock generator unit,

wherein said clock generator unit comprising:

a first control signal generator unit responsive to receipt of an input signal, for generating a first control signal for integral control of an output signal;

a second control signal generator unit for generating, based on the input signal, a second control signal for proportional control of an output signal;

an oscillator responsive to the first and second control signals for outputting a clock signal;

a first feedback circuit for feeding back an output of said oscillator to said oscillator through said first control signal generator unit; and

a second feedback circuit for feeding back an output of said oscillator to said oscillator through said second control signal generator unit,

wherein said first feedback circuit and said second feedback circuit are connected to said oscillator at all times so as to operate continuously, and

said second control signal generator unit includes a first converter circuit for conversion of an input signal to a first voltage, a second converter circuit for conversion of an output signal to a second voltage, and a voltage adder circuit for adding together said first voltage and said second voltage.